REMARKS

Claims 1-23 remain pending in the application. Claims 1, 3, 4, 6-11, 13 and 18 have been amended.

Claims 1-21 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Applicants have now amended Claims 1, 3, 4, 6-11, 13 and 18 to correct the stated insufficiency of antecedents.

As a result of the foregoing amendments, Applicants believe that the amended claims 1-21 are now free of rejection under 35 U.S.C. 112, second paragraph, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Claims 1, 3-12 and 23 stand rejected under 35 U.S.C. 102(e) as being anticipated by Patra et al. (U.S.P. 6,529,861 B1), (hereinafter referred to Patra).

Applicants traverse that stated rejection for the following reasons:

Petra teaches a method that is limited exclusively to domino logic. In column 5, lines 22-23, Petra explicitly states:

"The phase assignment only affects power consumption if the circuit is implemented in domino logic."

In contrast, Applicants submit that their teaching addresses how a phase assignment in conjunction with other steps reduces power consumption in scanning operations applicable to any logic network. Since Patra's teaching applies to a different type of logic operating in different ways, the architecture taught by Patra is believed to be unrelated to that of the Applicants.

Applicants submit that it is not possible to extrapolate, transfer or transport the teaching of a limited set of specialized circuits (i.e., domino logic) to any arbitrary logic, and much less to use an approach which, as taught by Patra, is valid mainly for combinatorial logic and fails to address sequential elements forming a scan chain.

The Office Action further rejects claim 3 under 35 U.S.C. 102(e) by citing lines 55-67 of column 3 of Patra which states the well known probabilistic equation that p(not x) = 1 - p(x). However, the Office Action fails to notice that Applicants' claim 3 refers not to probabilities of a signal being true or false, but instead to the probabilities that a stimulus value applied during a test to an arbitrary storage element matches the result value stored into the same storage element by a combinational logic network feeding it. This further reinforces the aforementioned argument that Patra addresses a totally different and unrelated invention to the one taught by the Applicants in the present application.

The Office Action rejects claim 4 under 35 U.S.C. 102(e) by citing that Patra teaches that the signal probability is the probability of a transition. The Office Action fails to consider that this assertion is only true and valid for domino logic, and is thus irrelevant to the present application. In contrast to Patra, the Applicants teach how to determine the probability of a change of the state of a storage element, i.e., the probability of the difference between a stimulus and a result value, which cannot be computed by any of the combinational logic probability computational methods taught by Patra, including the BDD based methods.

The Office Action rejects claims 5, 6, 7, 8, 9, 10 and 11 under 35 U.S.C. 102(e) by attempting to relate s1, s2, r1, and r2 in the Applicants claim to elements in the Figure 1 of Patra. However, the Applicants' specification clearly define a 'stimulus' to be understood as "a test pattern stimulus value loaded into a scannable storage element", and a 'result' is to be understood as "a value computed by a combinational logic network as input to a storage element". Thus, the connection which the Office Action makes between these terms and the elements illustrated in Figure 1 of Patra are not valid in the context of the present specification.

Accordingly, Applicants deem that the rejection of claims 1, 3-12 and 23 under 35 U.S.C. 102(e) over Patra et al. has been overcome, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

Claim 2 stands rejected under 35 U.S.C. 103(e) as being anticipated by Patra et al. (U.S.P. 6,529,861 B1) in view of Monteiro et al.

Referring to the rejection of claim 2 under 35 U.S.C 103(a), the Office Action cites a 1994 Design Automation Conference paper by Monteiro et al. which the Office Action states that it describes Applicants' set of random test patterns. Applicants contend that the test patterns referred to in the claims and described in the present specification pertain to tests patterns (also referred to test vectors), and not as described by Monteiro et al., as arbitrary random patterns specifically generated to estimate power consumption.

Applicants further teach away from Patra by making structural changes to the logic network by reordering scan chain elements. In contrast, Patra does not make structural changes, and instead maintains the same circuit structure while only changing the signal phases and gate functions.

The Office Action further rejects claims 14-17 and 19-22 as being unpatentable over Patra in view of Kajihara (CCAD 2001: 364-369).

With reference to claims 14-17, and 19-21, the Office Action states on page 8, last paragraph, that "Patra teaches the claimed invention described in claims 1, 3-12 (as rejected above)."

Applicants traverse this assertion for the reasons recited *supra*. Now, when Patra is combined with Kajihara, the combination fails to teach a phase assignment in conjunction with other steps reduces power consumption in scanning operations for arbitrary logic networks. Since Patra's teaching applies to different types of circuits operating in different ways (i.e., domino logic), Applicants contend that the teaching of Patra is unrelated to that taught by the Applicants.

The Office Action further rejects claim 22 under 35 U.S.C 103(a) stating that in lines 1-48 of column 7 Patra et al. describe reduction of scan switching. Applicants respectfully traverse this assertion. Patra teaches the use of partial scan flip-flops, but fails to mention the key element of the present invention, namely, architecting flip-flops into forming scan chains which are necessary to guarantee 100% test coverage.

The power reduction taught by Patra is limited to occur during combinational logic operations and not during scan operations. In fact, the rationale for the method steps taught by Patra is to allow insertion of flip-flops which do not have to be placed into scan chains (this is the meaning of partial scan flip-flops). In contrast, Applicants teach the reduction of power in flip-flops which are connected in a scan chain, specifically reducing the power dissipated during scan operations.

Furthermore, the connection of partial scan flip-flops into scan chains taught by Patra is performed based on the s-graph reduction described by Kajihara et al. in the reference cited, and is not based on value probabilities.

The combination of the Patra with the cited references thus fails to provide a methodology that reduces power consumption for any arbitrary logic wherein flip-flops are architected into scannable chains, and which being based on value probabilities.

Applicants therefore contend that claims 14-17 and 19-22 are patentable over Patra in view of Kajihara, and respectfully request that the rejection of the stated claims under 35 U.S.C. 103(a) be reconsidered and withdrawn.

In view of the foregoing amendments and arguments, Applicants respectfully request that all the rejections and objections to this application be reconsidered and withdrawn and that the Examiner pass all the pending claims to issue.

Respectfully submitted,
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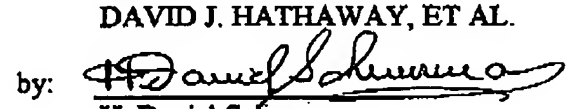
by: 

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